

IP Port TDR Seminar: Four Device Comparison

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IP Port Test & Model Objectives

- TDR (S11) measured to IC input Transceivers
- Partition TDR into exact component models (e.g. via)
- Optimize Hspice simulation to match S11 measurement
- Simulate TDT/S21 for 1ns eye diagram
- Differentiate IC performance by Eye & S Parameters
- Differentiate IC performance by S11/S21 crossover
- Use IConnect Analysis to convert Time Domain Simulations to Impedance, S parameters and Eyes
- Use Analysis to define network S11 Pass/Fail test

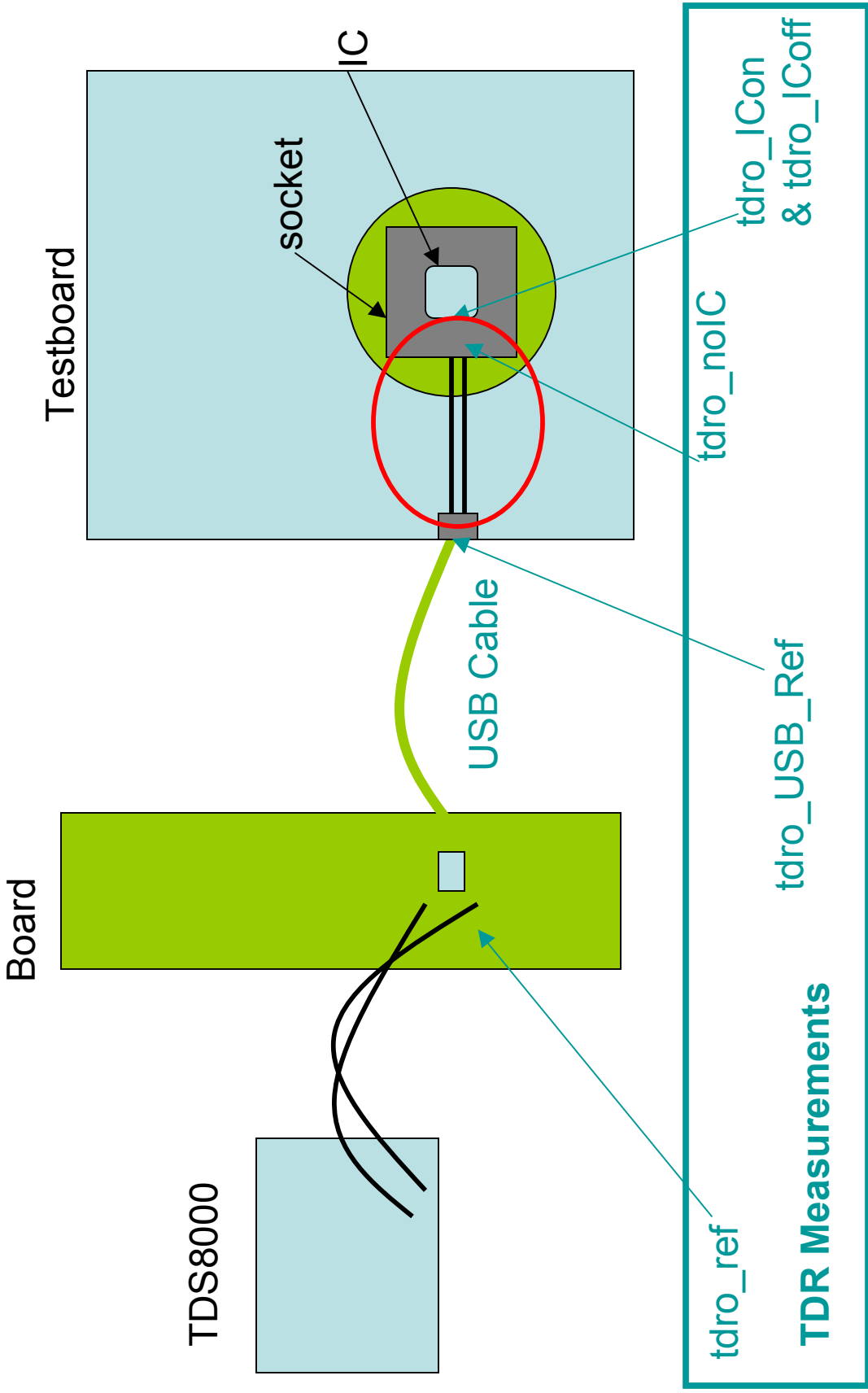
2 Port S Parameters From 1 Port TDR Test

With access to input TDR only, two port S parameters were extracted from “open termination” and “balance termination” TDR measurements. For this device the IC was actively terminated (on chip and down stream). The IC could be switched from a dc open to a 90 ohm differential (45 ohm single ended) termination. In the open state, the path length to the IC terminator was characterized. Then the device terminations were activated and differential Insertion and “true” Return loss was measured. S parameters were extracted from TDR’s to confirm exact accuracy. IConnect software can extract S parameters from Open TDR only.

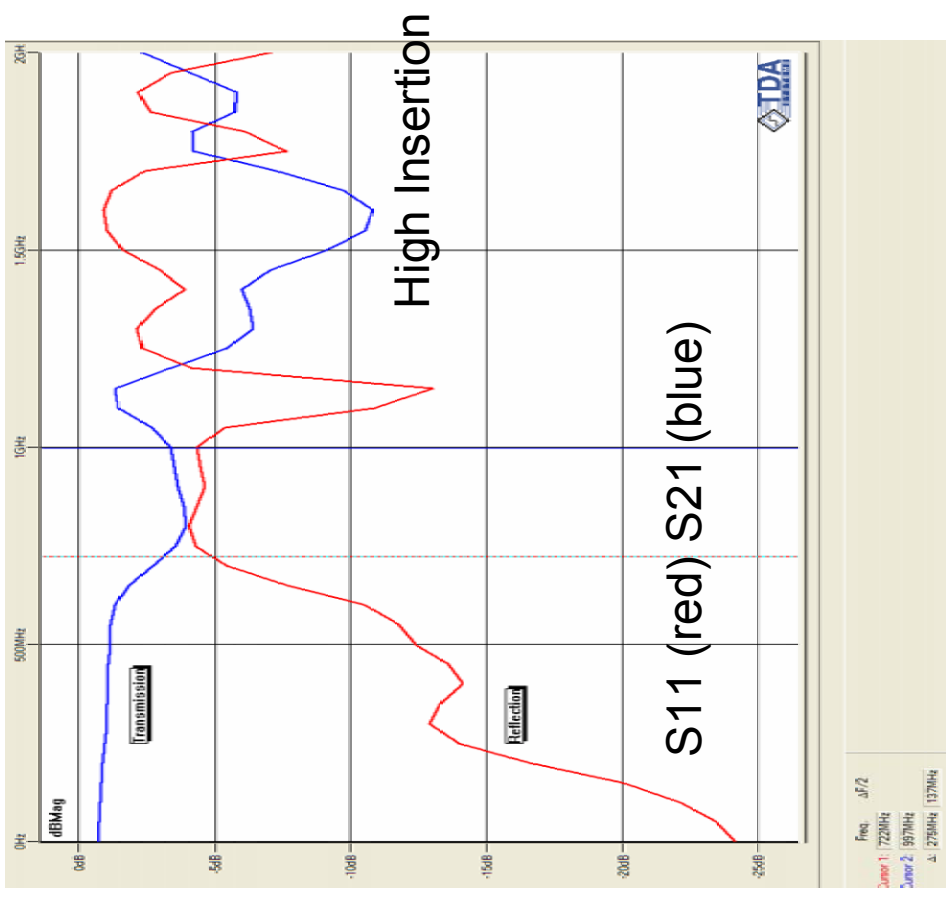
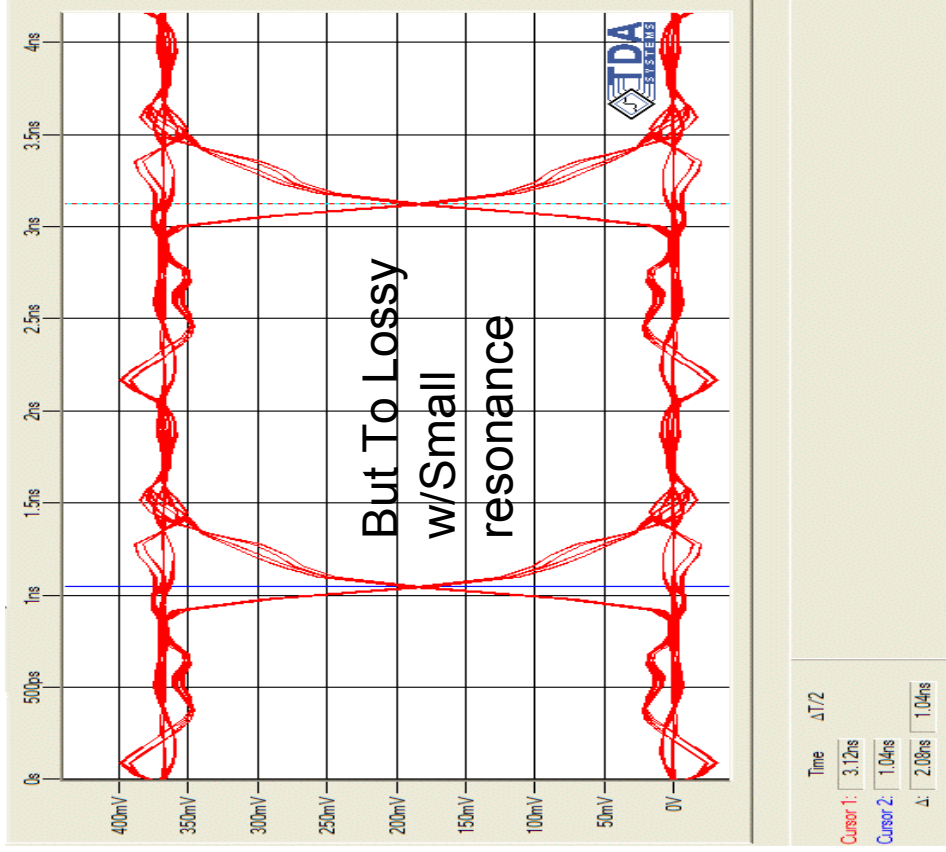
First IConnect software “un-peels” multiple TDR reflections creating a “true” impedance profile right into the IC input pin. The impedance measurement with active IP terminator was transformed to a “true” S11, return loss measurement. Open termination impedance profile was used to characterize for skin and dielectric loss by examining risetime degradation between input and open-reflection edges. Using IConnect a detailed spice model was created by SI engineer.

This was all done using IConnect & Hspice replacing open IC termination with active termination sub-circuit. 2nd Hspice simulation confirmed that IConnect had accurately “captured” the interconnect model which was then used to measure both Insertion (S21), return (S11) loss; plus hundreds of parameters such IC input capacitance to a fF accuracy.

USB Odd Measurement Locations



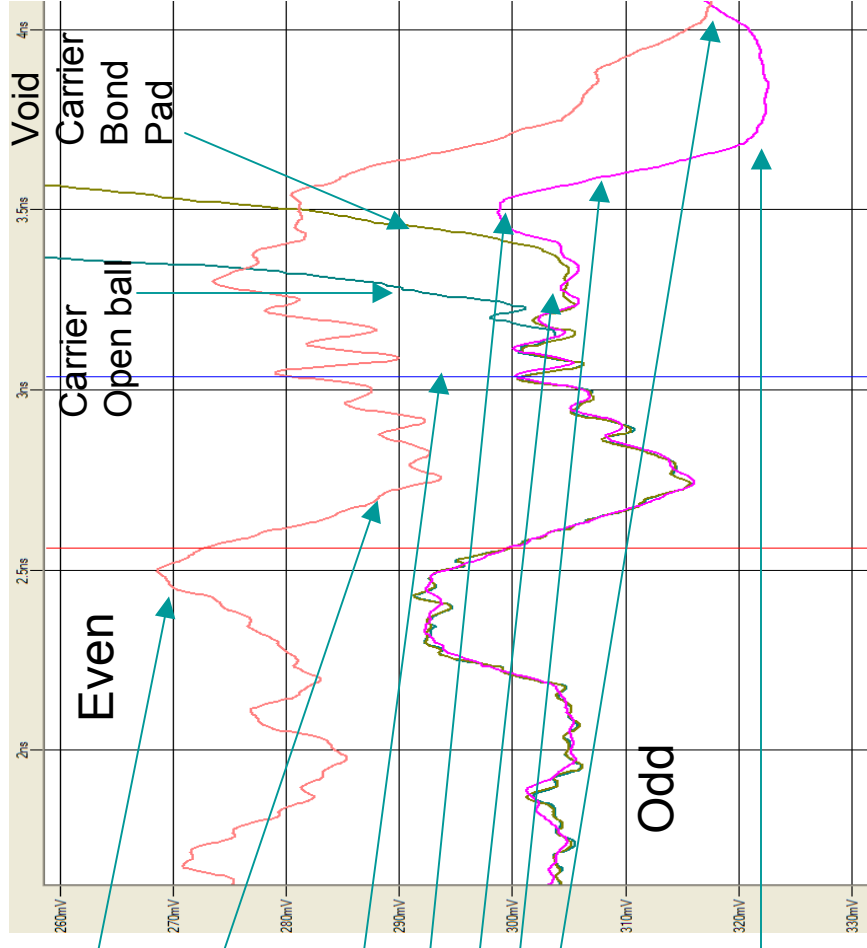
Package/IC1 Acceptible Risetime Height=400mv, Bit=2083ps



Even (common) & Odd(differential)

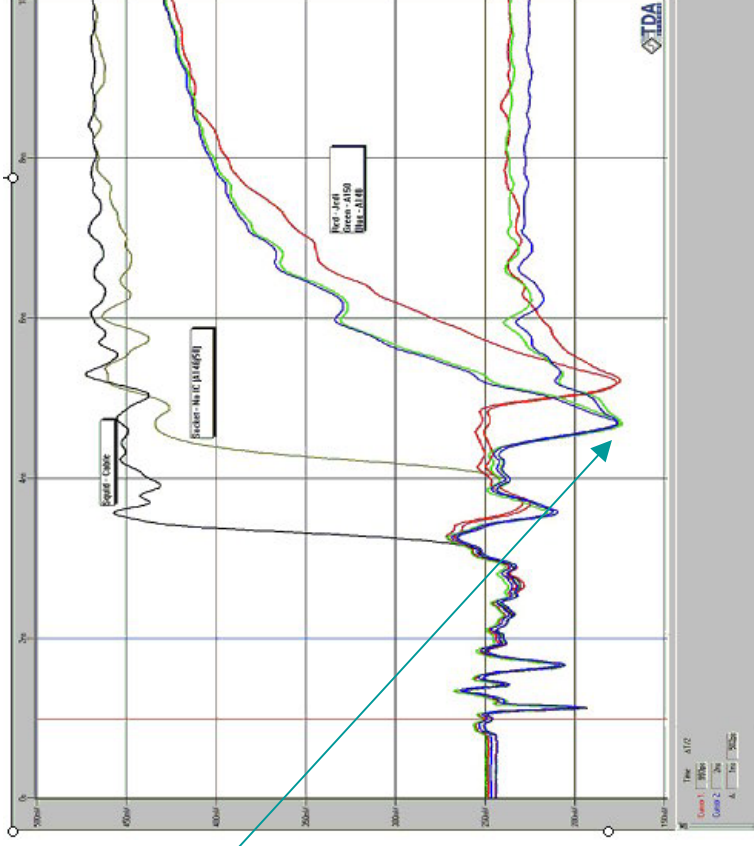
From Old TDR Data Defined partitions

- **Board:**
 - Module Zcommon +/-30% **marginal**
 - Due to Connector High Z
 - Due to Via Z Dip
 - Degradates:
 - Differential Z_{dd}
 - **Return Loss (SD11)**
- **Testboard**
 - Bond Wire Z **ok**
 - Chip Carrier Z **ok**
 - IC Input pad Capacitance **not ok**
 - The end at TDR (Even=Odd)
- **IC or PCB fix???**
 - Decrease IC input Cin by **half**
 - Or fix High Z discontinuities
 - Or fix both (not needed for **-10 dB S11**)



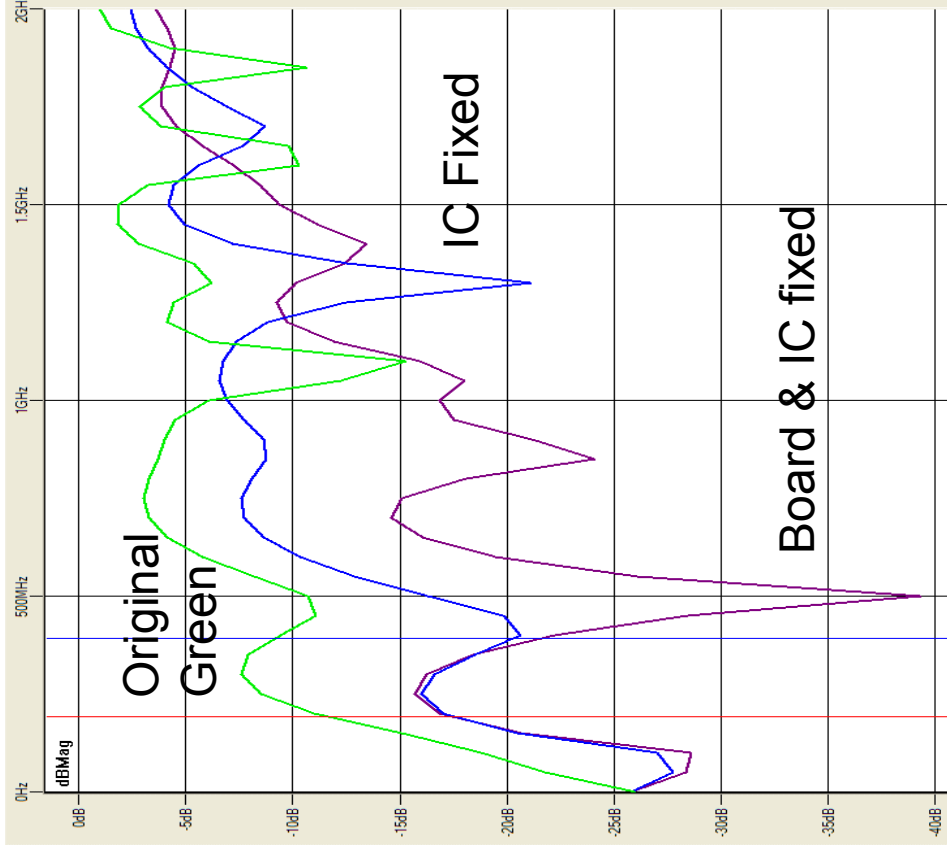
Determine pad/input capacitance From 30ps TDR Waveforms

- Pad Input Capacitance which has lowest Dip IConnect measures it
- See several effects?,
 - Si pad
 - IC Chip carrier
 - bondwire
- 30ps TDR Smears Data? **No**
- Enough Separation? **Yes**
- **Cin Dominates**



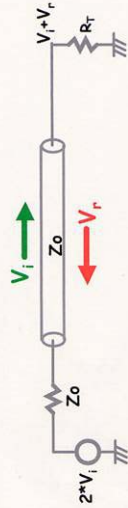
IC Versus Board S11 Plots

- Green return loss exceeds -5dB above 600 MHz. If IC impedance variation were limited to 10% with board unchanged then the return loss improves (blue) by 4 dB causing return Loss to pass.
- If board was also limited to a 10% variation, then Purple S11 >10 dB at 1 GHz!!!
- “IC” fix recommended



JDEC Notes On Gigabit S11

Return Loss Definition

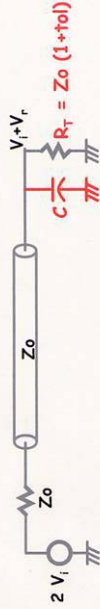


$$S_{11} = V_r / V_i$$

$$\text{Return Loss} = 20 \log_{10}(1/|S_{11}|)$$

$$\text{SDD11} = 20 \log_{10}(|S_{11}|)$$

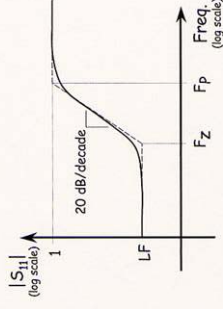
Return Loss Spec Format



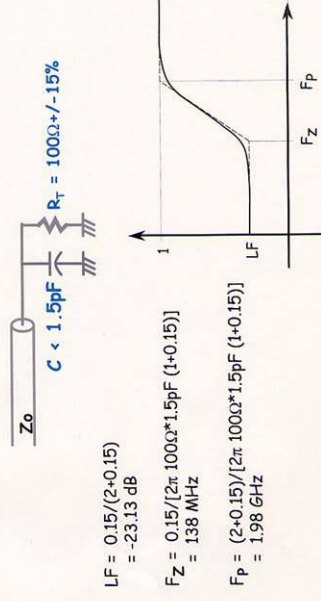
$$\text{LF} = \text{tol} / (2 + \text{tol}) \sim \text{tol} / 2$$

$$F_Z = \text{tol} / [2\pi R C (1 + \text{tol})] \sim \text{tol} / (2\pi R C)$$

$$F_P = (2 + \text{tol}) / [2\pi R C (1 + \text{tol})] \sim 1 / (\pi R C)$$



Proposed Return Loss Spec (1 of 2)

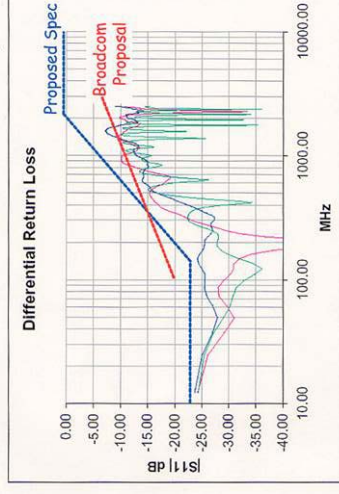


$$\text{LF} = 0.15 / (2 + 0.15) = -23.13 \text{ dB}$$

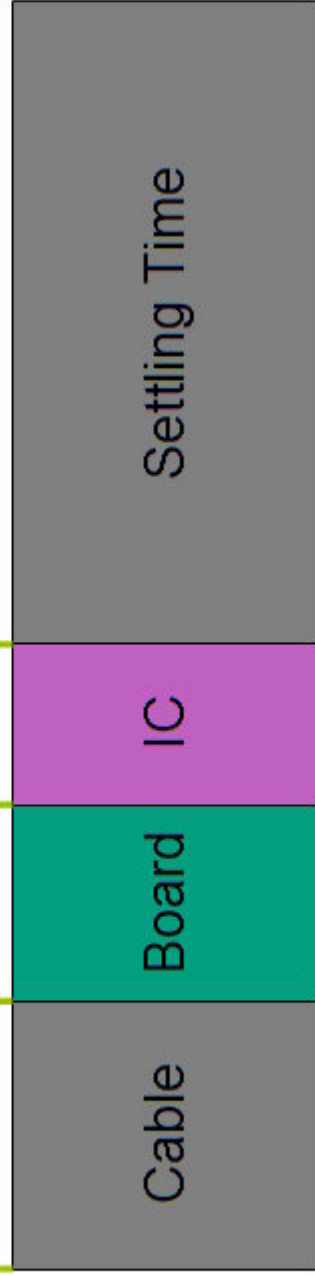
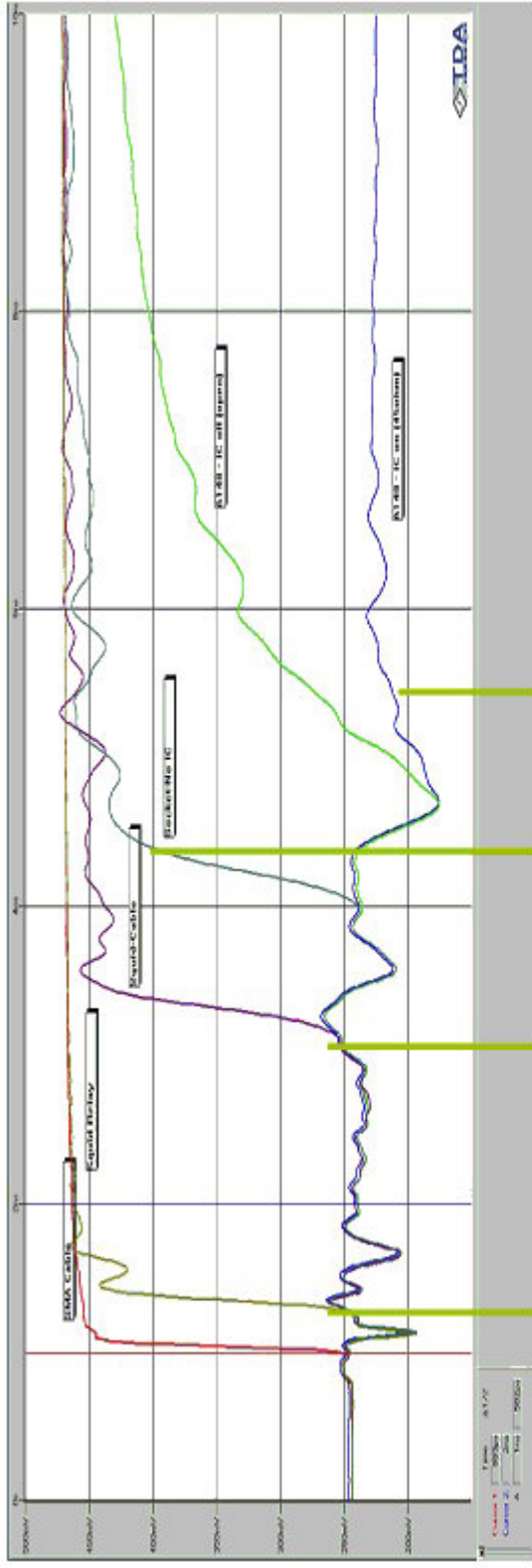
$$F_Z = 0.15 / [2\pi \cdot 100 \Omega \cdot 1.5 \text{ pF} (1 + 0.15)] = 138 \text{ MHz}$$

$$F_P = (2 + 0.15) / [2\pi \cdot 100 \Omega \cdot 1.5 \text{ pF} (1 + 0.15)] = 1.98 \text{ GHz}$$

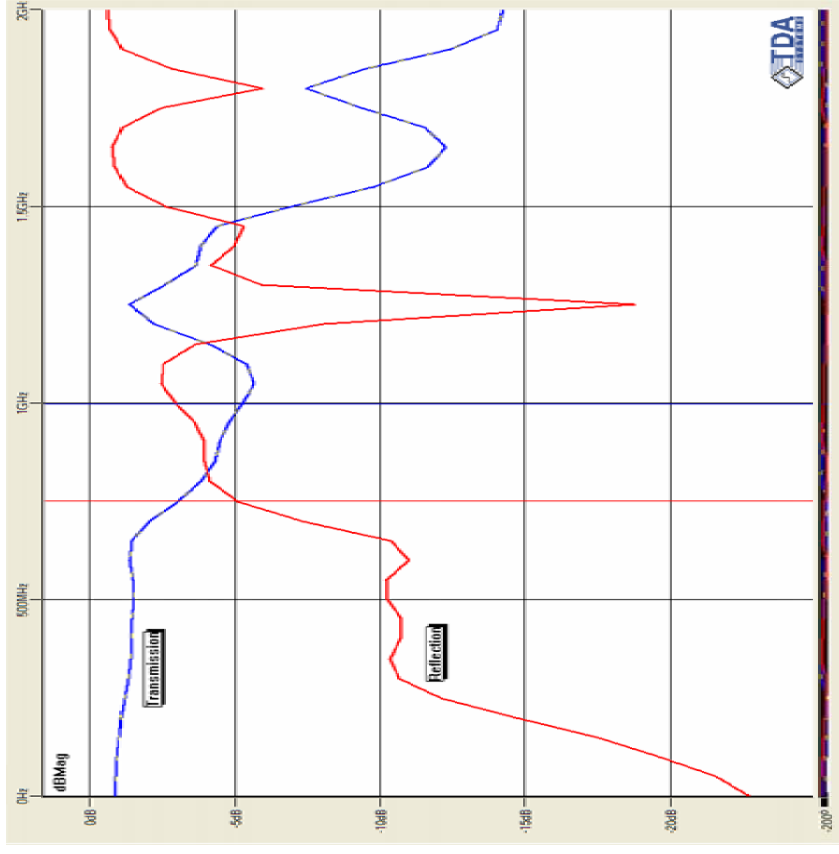
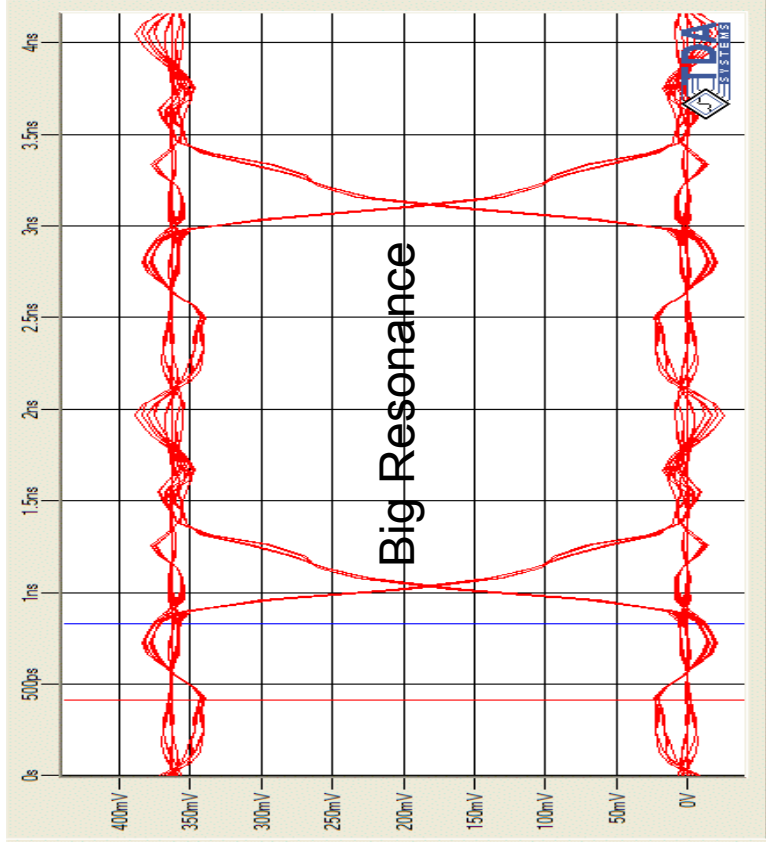
Return Loss: Data vs. Spec



USB CABLE, PCB IP IC INPUT Diff-TDR WAVEFORM



Package/IC2 S11 Resonance Height=400mv, Bit=2083ps



Time $\Delta T/2$

Cursor 1: 412ps

Cursor 2: 832ps

Δ : 420ps 210ps

Freq $\Delta f/2$

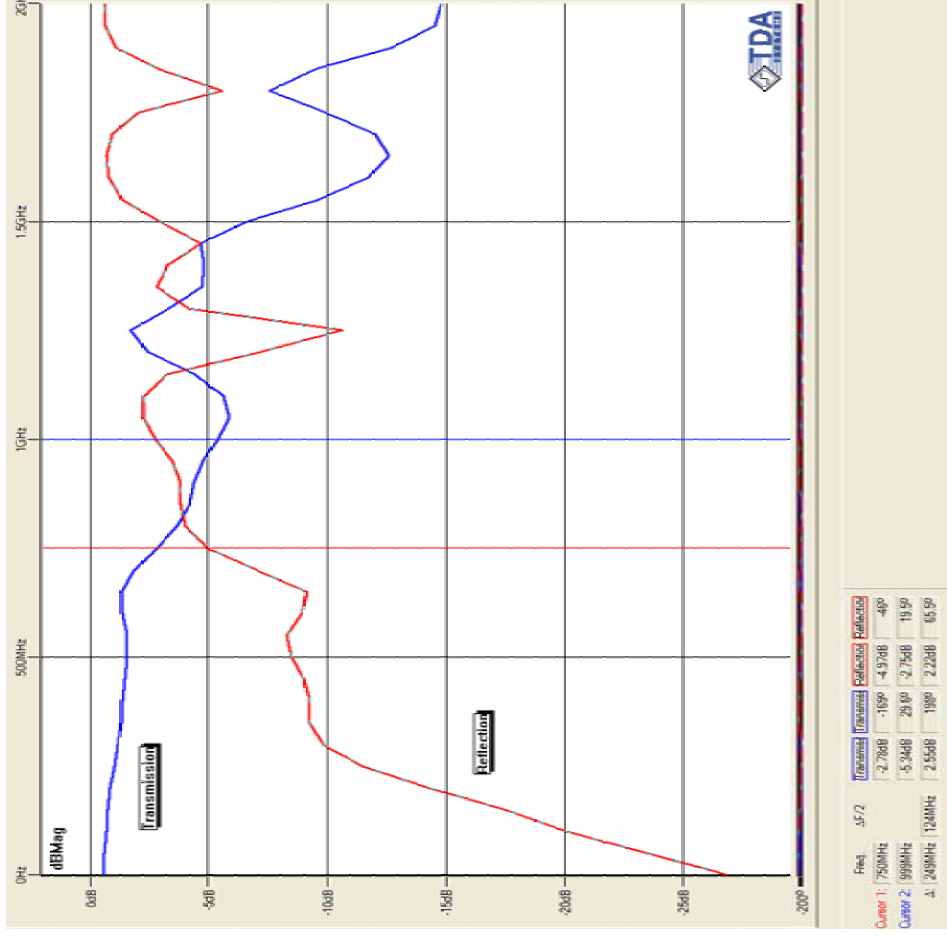
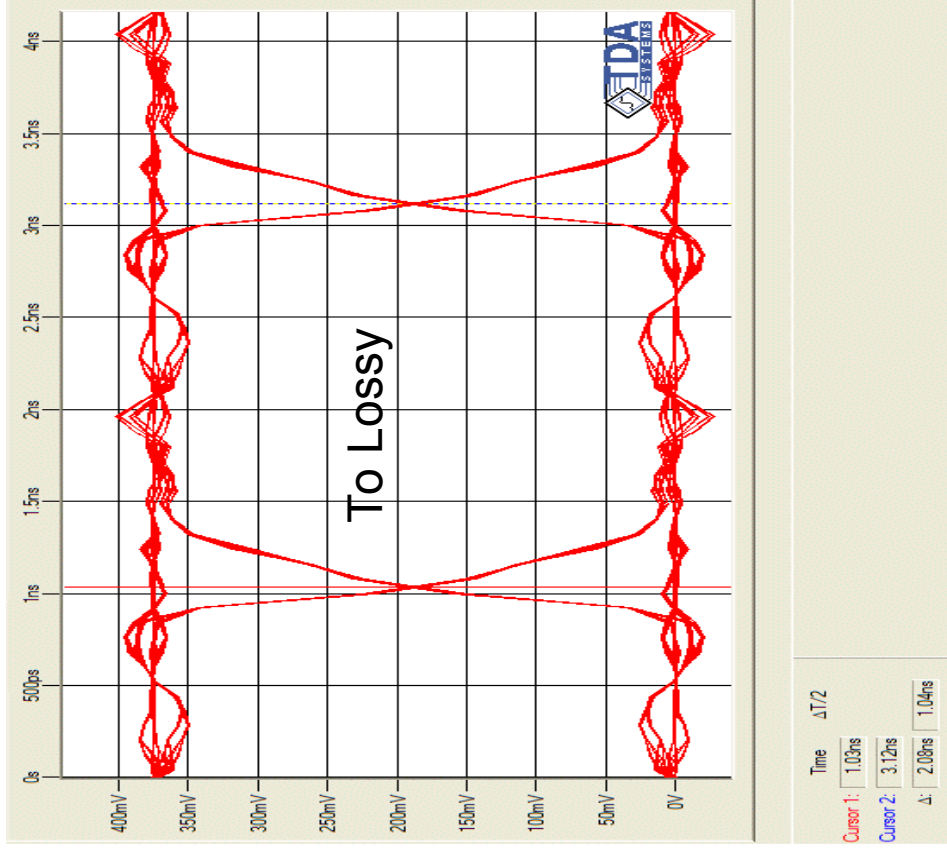
Reflection Reflection Transmission Transmission

Cursor 1: 750MHz -4.05dB -54.49 -3.08 -1779

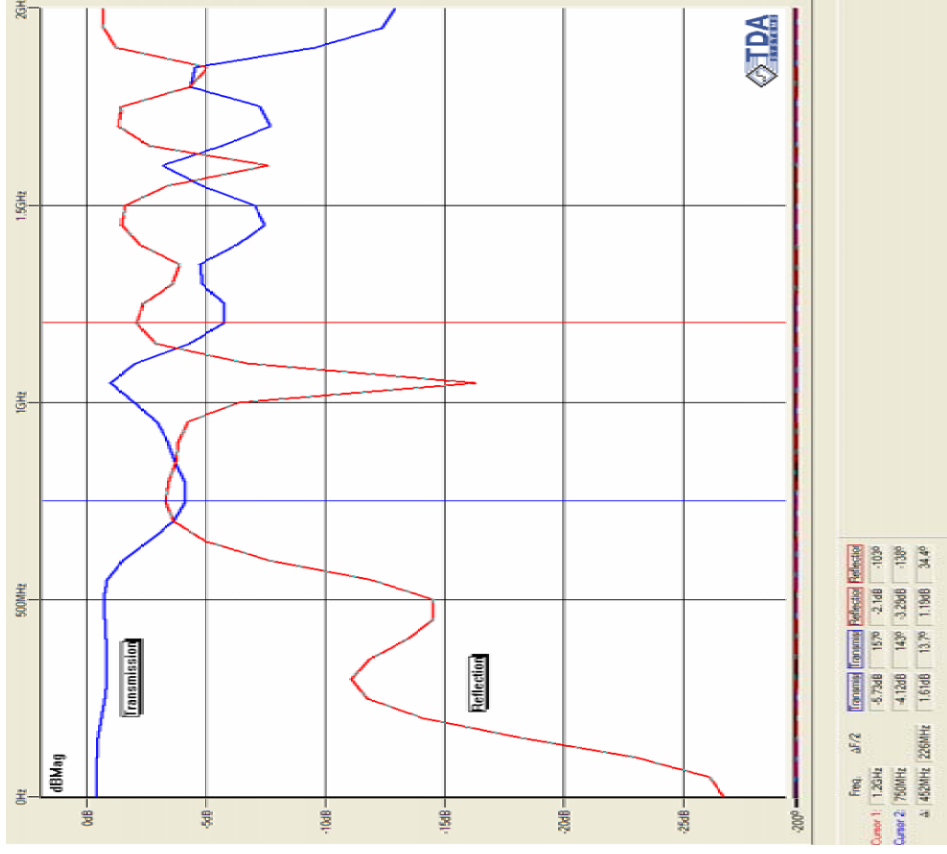
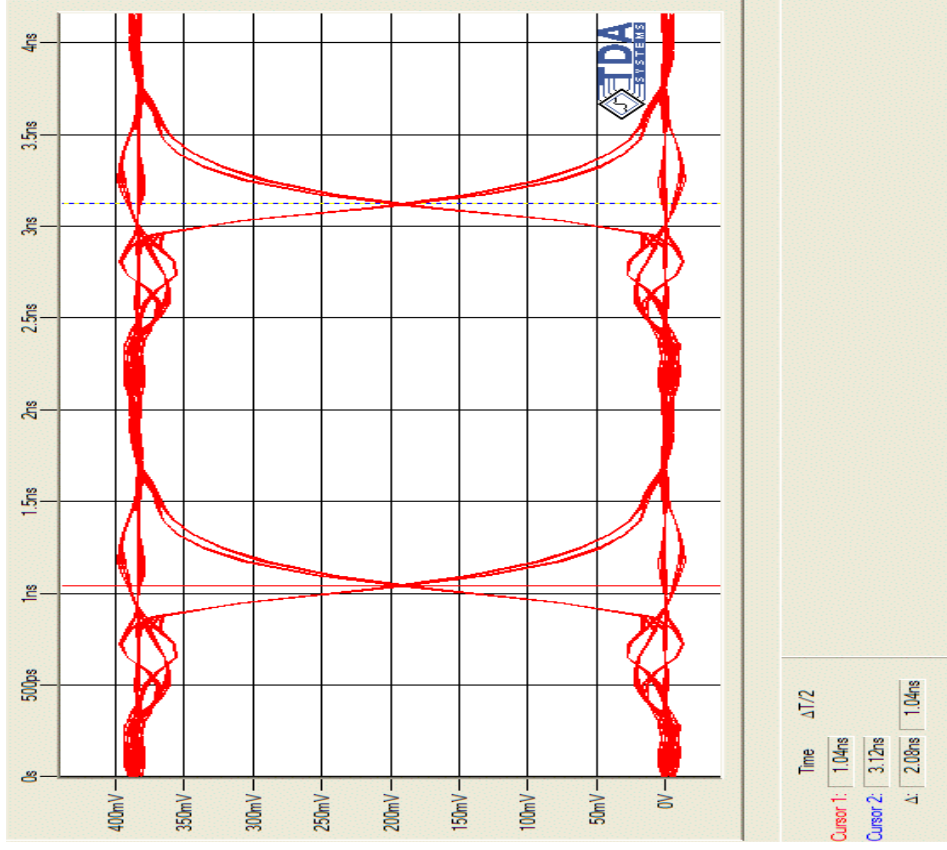
Cursor 2: 597MHz -3.86dB 29 -5.26dB 29.49

Δ : 246MHz 123MHz 2.11dB 78.39 2.74dB 2019

Package/IC3 Model Waveforms Height=400mv, Bit=2083ps



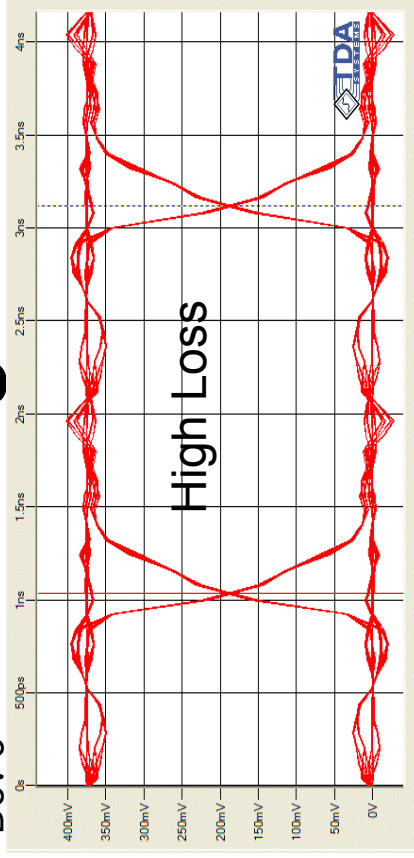
Package/IC4 Model Waveforms Height=400mv, Bit=2083ps



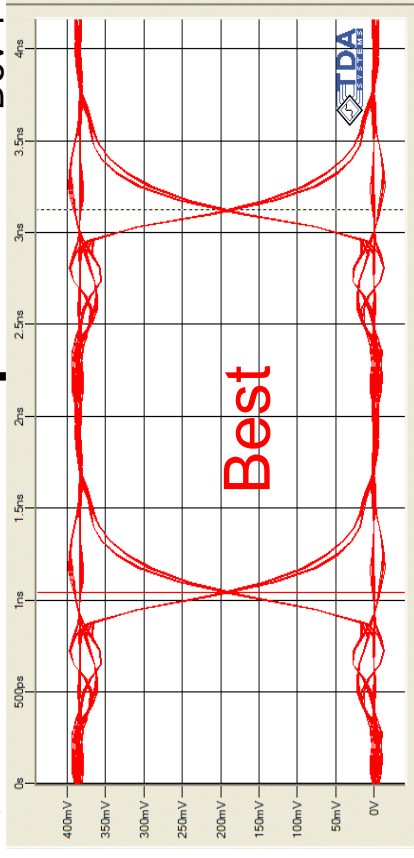
USB IP Device Eye Comparison

Height=400mv, Bit=2083ps

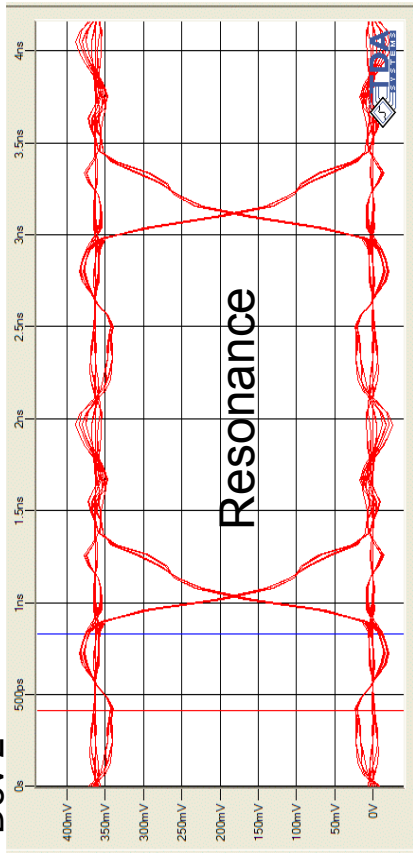
Dev 3



Dev 4



Dev 2



Dev 1

