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Utilizing TDR and VNA Data to Develop 4-port Frequency Dependent Models

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Abstract

Frequency dependent effects are becoming more prominent with the increasing data rates of digital systems. Differential circuit topology is proliferating throughout design laboratories with the goal of enhancing the data carrying capable of the physical layer. Simple impedance and delay measurements of copper transmission lines on backplanes are not sufficient to ensure accurate analysis of gigabit interconnects. The challenge to push design rules to the limit now requires the use of concurrent time and frequency domain analysis. This paper will discuss methods to achieve proper characterization using a Time Domain Reflectometer (TDR) oscilloscope and Vector Network Analyzer (VNA). Measurement accuracy and error correction techniques will be discussed for both time domain and frequency domain instrumentation. It will be demonstrated that accurate 4-port frequency dependent models can closely simulate performance of a differential channel.

Jim Mayrand

Jim Mayrand is an independent signal integrity consultant operating offices in San Francisco and Massachusetts. He has extensive backplane and ASIC design experience with in-depth knowledge of both interconnect and IC device physics. Prior to retiring from Hewlett Packard as a hardware design engineer, he worked in the semiconductor product test and design engineering field. Jim has a novel perspective of signal integrity in tribute to his practical understanding of copper interconnect having worked his way through college as journeyman electrician. Jim received a Masters of Science Degree from University of New Hampshire in Electrical Engineering and holds four patents.

Mike Resso

Mike Resso is a Product Manager in the Signal Integrity Operation of Agilent Technologies. He is responsible for technical training of Agilent field engineers and interfacing with Agilent R&D engineers to bring innovative products to market. Mike has over twenty years of experience in the test and measurement industry and has focused on understanding signal integrity issues from both time domain and frequency domain perspectives. His most recent activity includes developing application techniques for complete 4-port characterization utilizing Time Domain Reflectometry (TDR) and Vector Network Analysis (VNA). He has experience in the design and development of electro-optic test instrumentation and has published numerous technical papers. Mike received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Dima Smolyansky

Mr. Smolyansky has spent his professional career in the instrumentation and measurement industry working with high-speed time domain reflectometry oscilloscopes and frequency domain network analyzers. He is currently working on application development for model extraction tools that enhance signal integrity and high-speed digital design work. During his professional career, Mr. Smolyansky has accumulated significant experience in the area of high-speed digital interconnect measurements and modeling. He has published a number of papers and taught short courses on interconnect analysis. Dima received a Masters of Science Degree from Oregon State University and the Engineer Diploma (M.S.) degree from Kiev Polytechnic Institute.

Signal Integrity Challenges

With the increase in speed of digital system design into the gigahertz region, frequency dependent effects become a more prominent challenge than in the past. Yesterday's interconnects could be easily characterized by measuring the self impedance and propagation delay of the single-ended transmission line. This was true for printed circuit board stripline, microstrip, backplanes, cables and connectors. However, the proliferation of high speed serial data formats in today's digital standards demand differential circuit topology. A paradigm shift in measurement technology is required to achieve the design goals of the advanced differential physical layer. It is now necessary to consider both time and frequency domain analysis to obtain proper characterization. Tracking the technology adoption curve in Figure 1 below, it can be seen that several new implementations of PCI Express and Infiniband reach data rates into the 4 Gb/sec range. New standards, such as XAUI, OC-192, 10G Ethernet, and OC-768 aim even higher—up to and past 40 Gb/sec. This upward trend creates signal integrity challenges for physical layer device designers and the inevitable struggle to keep up with data processing and storage capabilities.

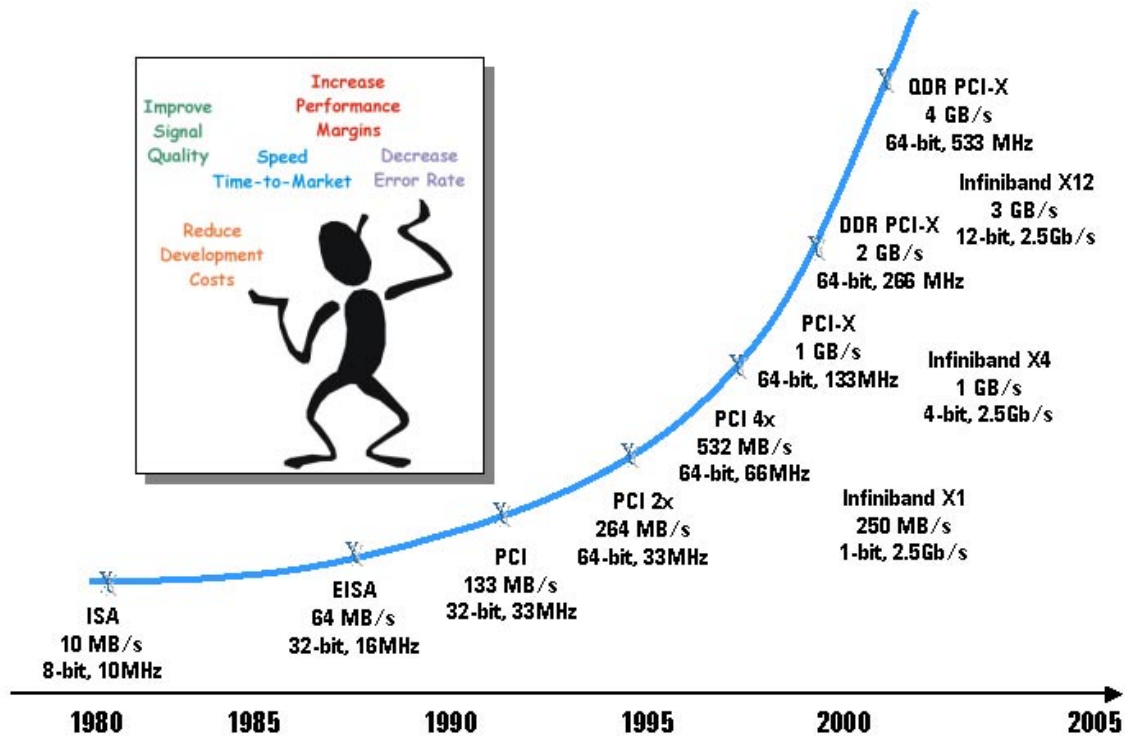


Figure 1. Partial list of many new high-speed serial link formats

Trend to Differential Topologies

In the discussion of these new signal integrity challenges, it becomes clear why we need to understand the implications of differential topologies and how mode-conversion analysis is an important concept for designing digital interconnects.

Ideal differential linear passive interconnects respond to and/or generate only differential signals (two signals of equal amplitude and opposite polarity). These perfectly designed devices exhibit beneficial characteristics noted in Figure 2 and do not generate in-phase

signals (a.k.a. common mode signals). Any radiated external signal incident upon this ideal differential transmission line is considered a common signal and is rejected by the device. This is called Common Mode Rejection Ratio (CMRR) and is the main benefit of differential topology. The radiated common signals are usually generated from adjacent RF circuitry or from the harmonics of digital clocks. Properly designed differential devices can also reject noise on the electrical ground, since the noise appears common to both input terminals.

Non-ideal differential transmission lines, however, do not exhibit these benefits. A differential transmission line with even a small amount of asymmetry will produce a common signal that propagates through the device. This asymmetry can be caused by any physical feature that is on one line of the differential pair and not the other line, including solder pads, jags, bends and digs. This mode conversion is a source of EMI radiation. Most new product development must include EMI testing near the end of the design cycle. Very often the test results show that the design exhibits EMI radiation or susceptibility. However, there is usually very little insight as to what physical characteristic is causing the EMI problem. Mode conversion analysis provides the designer with that insight so that EMI problems can be resolved earlier in the design stage.

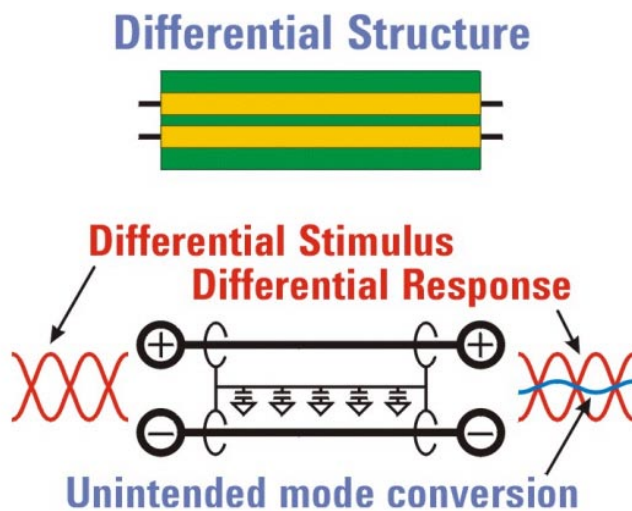


Figure 2. Ideal differential structures exhibit no mode conversion is they are perfectly symmetric

Model Extraction Methodologies

In order to describe the test system laboratory configuration used in this design case study, the authors will refer to the flowchart in Figure 3 for clarification purposes. Measurement based model extraction can be accomplished using a variety of methods. Starting from the top, the goal is to achieve an accurate model that can be simulated in either the time domain or frequency domain. Most digital designers will focus on time domain models and that will be our focus in this paper, also. Either a topological model or behavioral model maybe developed. The topological model is based on the physical structure of the device and can be very complex for a lengthy device exhibiting multiple impedance discontinuities. This requires multiple iterations and is easily done using today's standard PC computational power. The behavioral model is a "black box"

approach and describes how the device behaves toward a particular stimulus. One type of behavioral model is scattering parameters or S-parameters.

This flowchart shows that both time domain test equipment (Time Domain Reflectometer or TDR) and frequency domain test equipment (Vector Network Analyzer or VNA) were used to measure prototype devices. Both test instrument types have strengths and weaknesses and the specific user application will normally dictate the use of one or the other. In general, the TDR is easier to use and the VNA is more accurate. Most signal integrity laboratories have one of each.

In this experiment, measurements were made with a VNA using the Agilent N1930A Physical Layer Test System software to control the VNA via GPIB. This allowed for use of the automated calibration wizard and simplified this typically rigorous and error prone process. The resultant 4-port S-parameter data was exported to the TDA Systems IConnect MeasureXtractor model extraction tool that in turn created an accurate time domain Hspice model.

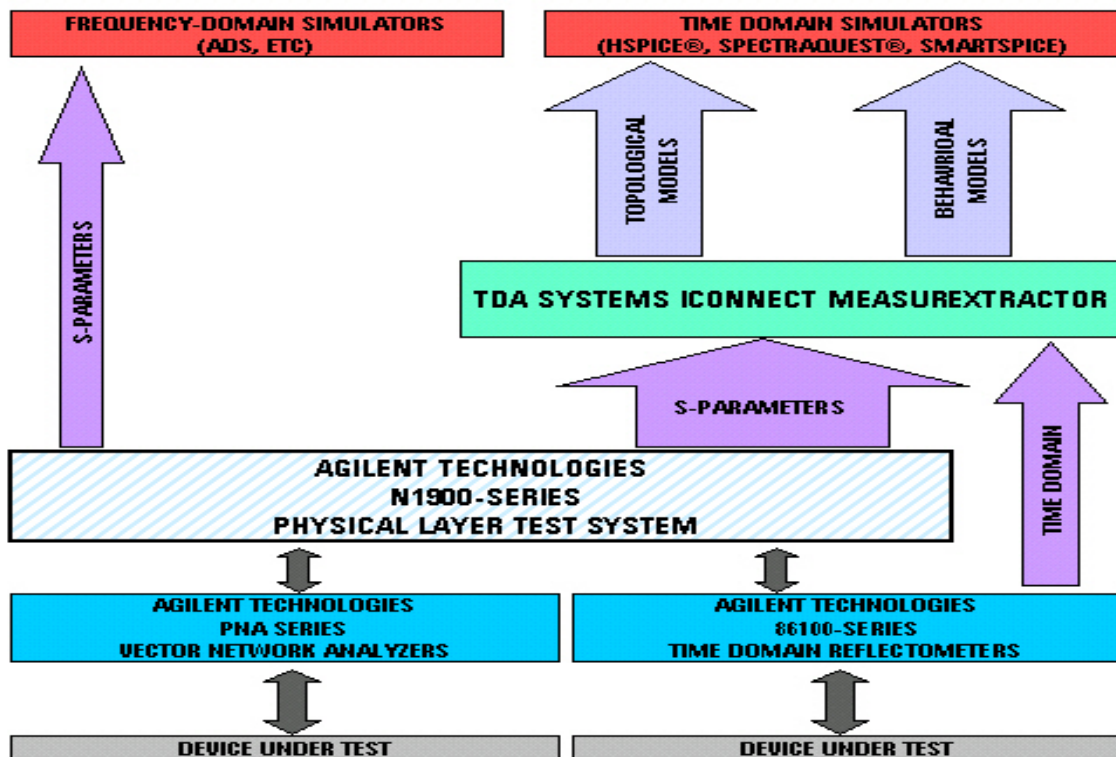


Figure 3. Many different methods exist today for model extraction, but measurement-based model extraction is a relatively new process yielding insight into high frequency effects.

The model extraction tool used in this design case study was the TDA Systems IConnect MeasureXtractor. It was chosen because it was simple and easy to use. This extraction tool imports the impedance profile or 4-port S-parameters after the user performs the measurement with either a Time Domain Reflectometer (TDR) or Vector Network Analyzer (VNA). The resultant model can be directly linked to a simulator subsequent to using a laptop to perform multiple iterations of model refinement. The convenience of comparing measured results to simulated results very quickly is an efficient way to check accuracy of models.

Typical Four Port Measurement Systems

Measurement based models for differential devices require a 4-port measurement system. A well-calibrated and controlled stimulus will be input to the device under test and the response will be measured with receivers co-located within the same measurement system. With a full 4-port measurement system, this stimulus/response test is performed on the reflected response and transmitted response in both single-ended mode and differential mode. The TDR instrument accomplishes this task with a fast step with little overshoot in concert with a wideband receiver to measure step response. The VNA uses a precise sine wave and sweeps frequency as a narrow band receiver tracks the swept input response. This narrow band receiver is what enables low noise and high dynamic range of the VNA.

Whether the data acquisition hardware is time domain based or frequency domain based, mixed mode data is also compiled in a 4-port measurement system. The mixed mode data refers to two specific test conditions: one being differential stimulus and common response and the other being common stimulus and differential response. This analysis leads to the discovery of interesting effects due to asymmetry within a differential transmission line.

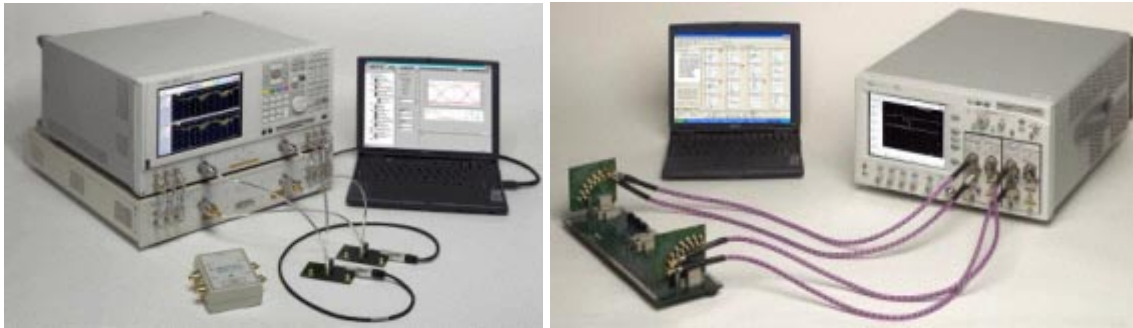


Figure 4. High-speed differential interconnects need to be characterized with a 4-port measurement system, whether it be a 4-port VNA (left) or 4-channel TDR (right).

Understanding 4-port Mixed Mode Analysis

In order to interpret the large amount of data in the differential parameter matrix, it is helpful to analyze one quadrant at a time. The first quadrant is defined as the upper left 4 parameters describing the differential stimulus and differential response characteristics of the device under test. This is the actual mode of operation for most high-speed differential interconnects, so it is typically the most useful quadrant that is analyzed first. It includes input differential return loss (SDD11), input differential insertion loss (SDD21), output differential return loss (SDD22) and output differential insertion loss (SDD12). Note the format of the parameter notation SXY_{ab} , where S stands for Scattering Parameter or S-Parameter, X is the response mode (differential or common), Y is the stimulus mode (differential or common), a is the output port and b is the input port. This is typical nomenclature for frequency domain scattering parameters. All sixteen differential S-Parameters can be transformed into the time domain by performing an Inverse Fast Fourier Transform (IFFT). The matrix representing the time domain will have similar notation, except the “S” will be replaced by a “T” (i.e. TDD11).

The second and third quadrants are the upper right and lower left 4 parameters, respectively. These are also referred to as the mixed mode quadrants. This is because they fully characterize any mode conversion occurring in the device under test, whether it is common-to-differential conversion (EMI susceptibility) or differential-to-common conversion (EMI radiation). Understanding the magnitude and location of mode conversion is very helpful when trying to optimize the design of interconnects for gigabit data throughput.

The fourth quadrant is the lower right 4 parameters and describes the performance characteristics of the common signal propagating through the device under test. If the device is design properly, there should be minimal mode conversion and the fourth quadrant data is of little concern. However, if any mode conversion is present due to design flaws, then the fourth quadrant will describe how this common signal behaves.

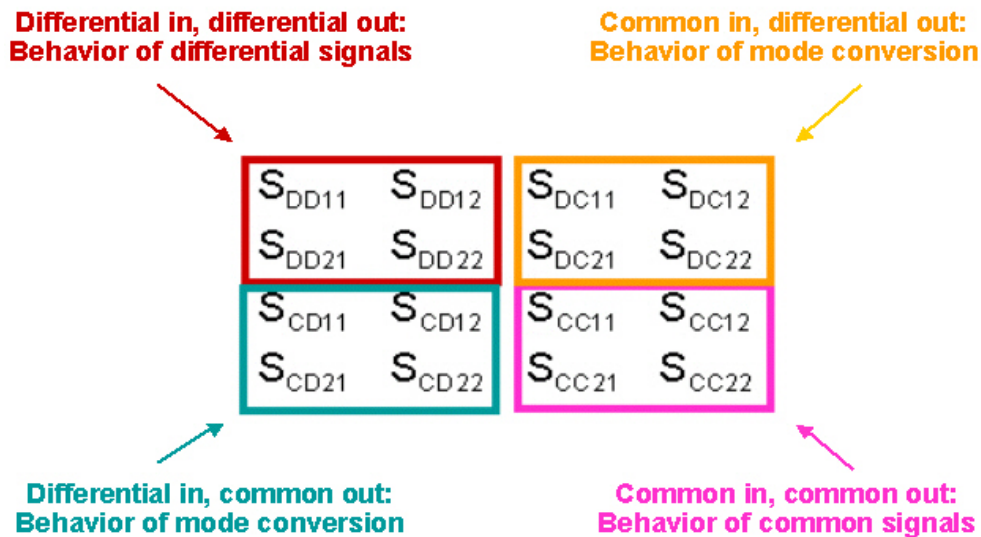


Figure 5. The sixteen S-parameters that are obtain by fully characterizing a differential interconnect can be categorized into 4 stimulus/response quadrants: differential in/differential out, common in/common out, common in/differential out and differential in/common out.

Differential Interconnect Analysis

Figure 6 describes the flow gram of the test and measurement methodology used in the backplane characterization. The first step in the process is to understand the 16 S-parameters and what information can be extracted from the sometimes overwhelming amounts of data. Next, the actual measurement is made to obtain these 16 S-parameters. This can be done with a variety of frequency domain instrumentation (vector network analyzers) or time domain instrumentation (time domain reflectometers). Then, finding the amount of losses in transmission lines by observing the input differential insertion loss (S_{DD21}) is important. This will give a very accuracy indication of the bandwidth of the device under test. Lastly, carefully analyzing mode conversion is desirable to high speed design. For example, pinpointing via field mode conversion in Figure 6, optimization of the design can be accomplished by determining the magnitude of mode conversion as a percentage of input signal and then locating the physical structure that is causing the mode conversion. One optional analysis that is sometimes interesting is

viewing reciprocity. By viewing the forward transmission and reverse transmission data, masking effects of TDR can be removed to clarify directional information.

Measure Important Parameters	
T_{DD11}	differential impedance profile
S_{DD21}	Signal quality of differential signal, time delay of differential signal
T_{CD11}	Conversion of differential signal to common signal in reflection (emissions)
S_{DC21}	Conversion of common signal to differential signal in transmission (susceptibility)
T_{CC11}	Common impedance profile
S_{CC21}	Signal quality of the common signal, time delay of common signal

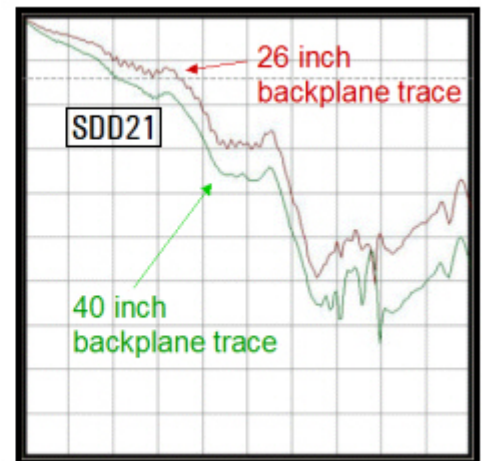
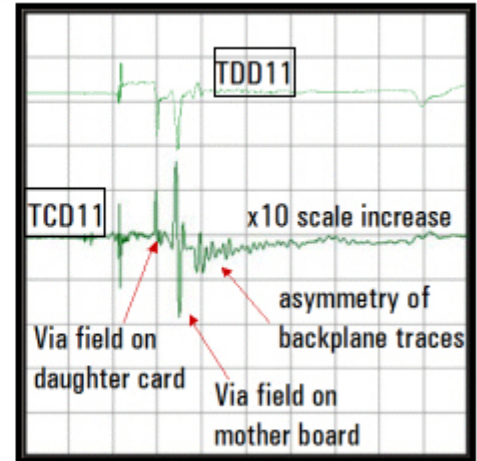


Figure 6. Example of typical 4-port analysis using both time and frequency domain data. Note: this just an example is from a 3Gb/s backplane, not from the design case study device.

Measurement Accuracy and Error Correction

Ideally, all test equipment would not require any correction. However, in the real world imperfections exist in even the highest quality test equipment. Some of the factors that contribute to measurement error are predictable over time and can be removed, while others are random and cannot be removed. The basis of error correction is to measure a known and understood electrical standard and use this device as a reference.

All measurement systems can exhibit three types of measurement error:

- Systematic errors
- Random errors
- Drift errors

Systematic errors are caused by imperfections in the test equipment and test setup. If these errors do not vary over time, they can be characterized through calibration and

mathematically removed during the measurement process. Random errors vary randomly as a function of time. Since they are not predictable, they cannot be removed by calibration. The main contributors to random errors are instrument noise. Drift errors occur when a test system's performance changes after a calibration has been performed. They are primarily caused by temperature variation and can be removed by additional calibration.

The error correction techniques shown in Figure 7 are described as follows: Time-Domain Gating is easiest to implement. The user defines a start and stop point, and software mathematically replaces the measured data in that section with an ideal transmission line. With the enhanced dynamic range of the network analyzer, multiple gates are possible, but accuracy diminishes in proportion to the number of gates. Port Extension will mathematically extend the measurement plane to the input of the device under test. However, it assumes the fixture looks like a perfect transmission line with a flat magnitude response, a linear phase response, and constant impedance. Port extensions are usually done after a coaxial calibration has been performed at the end of the test cables. De-Embedding removes a fixture or unwanted structure from the measurement by using the S-parameters or an accurate linear model of the structure. This S-parameter or model representation is mathematically removed from the DUT measurement data in post-processing. Calibration at the DUT Reference Plane has the advantage that the precise characteristics of the fixture don't need to be known beforehand, as they are measured during the calibration process. While calibration is the technique specific to Vector Network Analyzers, the normalization is the extension of the same procedure to the TDR oscilloscopes.

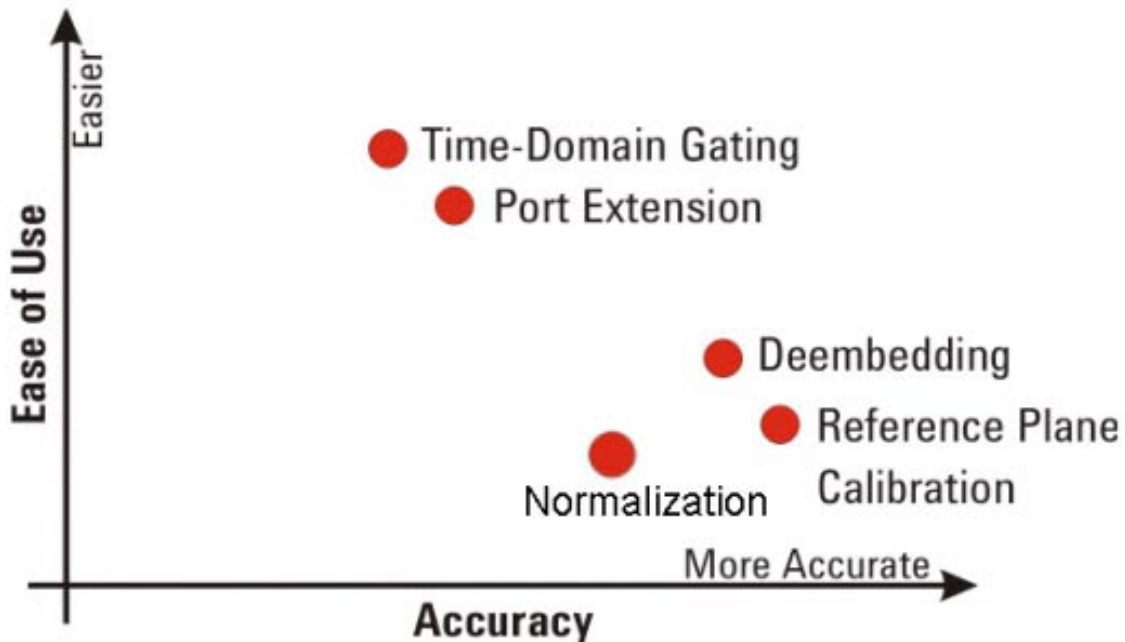


Figure 7. Various mathematical computations and error correction techniques can be made to enhance measurement accuracy. Usually, ease of use and degree of accuracy are inversely proportional to each other.

Design Case Study: Silicon Pipe ChannelPlane

The design case study described in the forthcoming analysis employed the use of a prototype provided by Silicon Pipe of San Jose. The ChannelPlane technology developed by Silicon Pipe creates a well-controlled impedance environment in the area surrounding the backplane/connector interface. Using a process conceptually analogous to optical fiber splicing where the two ends of a fiber are highly polished to achieve a closely matched index of refraction to minimize optical reflections, the ChannelPlane cross sectional copper conductors are polished to minimize electrical reflections. This results in a flush mount cable assembly compatible with the popular 2 millimeter Winchester SIP-1000 backplane connector. The prototype ChannelPlane cable was constructed from high bandwidth Gore G4 material that was cut three inches from the SMA end and terminated with a patented coax/twinax flush mount termination. A coaxial interposer was then used to mate to the Silicon Pipe coax cable. A picture of the ChannelPlane assembly with flush mount termination is shown in Figure 8. A functional block diagram in Figure 9 shows the construction details.

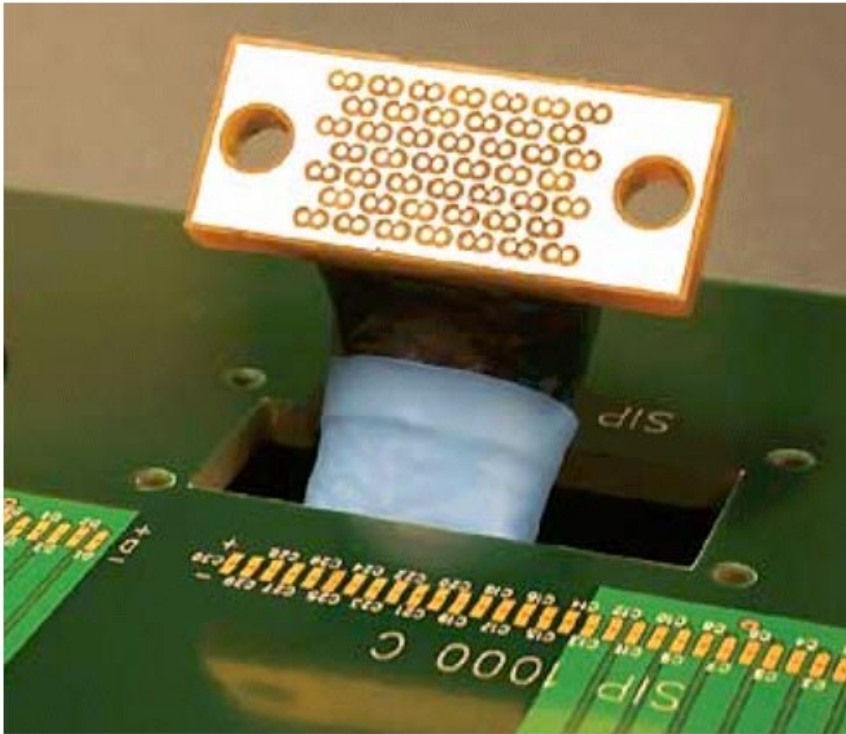


Figure 8. The Silicon Pipe ChannelPlane shown above is a backplane cable assembly that consists of a flush mount connector compatible with the Winchester SIP-1000 backplane connector



Figure 9. The Silicon Pipe ChannelPlane functional block diagram shows construction details

Frequency and Time Domain Analysis

There are many ways to develop models for digital interconnects. The first method used in this design case study is shown in the chart in Figure 10. Measurement based models constructed in this process combine precision 40 GHz VNA-PLTS testing with IConnect modeling, optimization and test correlation technique. This method is capable of resolving femtoFarads over 1/10mm distances even on long cables because of the nature of the VNA instrument. Time Domain Reflectometry testing, preferred for device model partitioning of paths, can be combined with VNA measurements to resolve small backplane connectors over long distances. In fact, field solver S-parameter output can also be used to resolve the issue of small devices in large system paths.

Frequency and time base correlation was required because of the large bandwidth and dynamic range required for this test. It was important to isolate and test coaxial lines with an 80dB accuracy in order to optimize impedance, insertion and return loss models. The model discovery process requires the ability to detect changes in impedance, risetime and frequency in small connectors embedded in long cables. For short electrical length devices, it is desired to have a test bandwidth of 80 GHz using a 7 ps Gaussian input pulse. Where system geometric dynamic range is large, it becomes easier to detect and optimize measurement-based models within the model extraction tool fitting measurements to Hspice simulations right in the laboratory. This is a more efficient way to discover, study and optimize the interaction between model attributes.

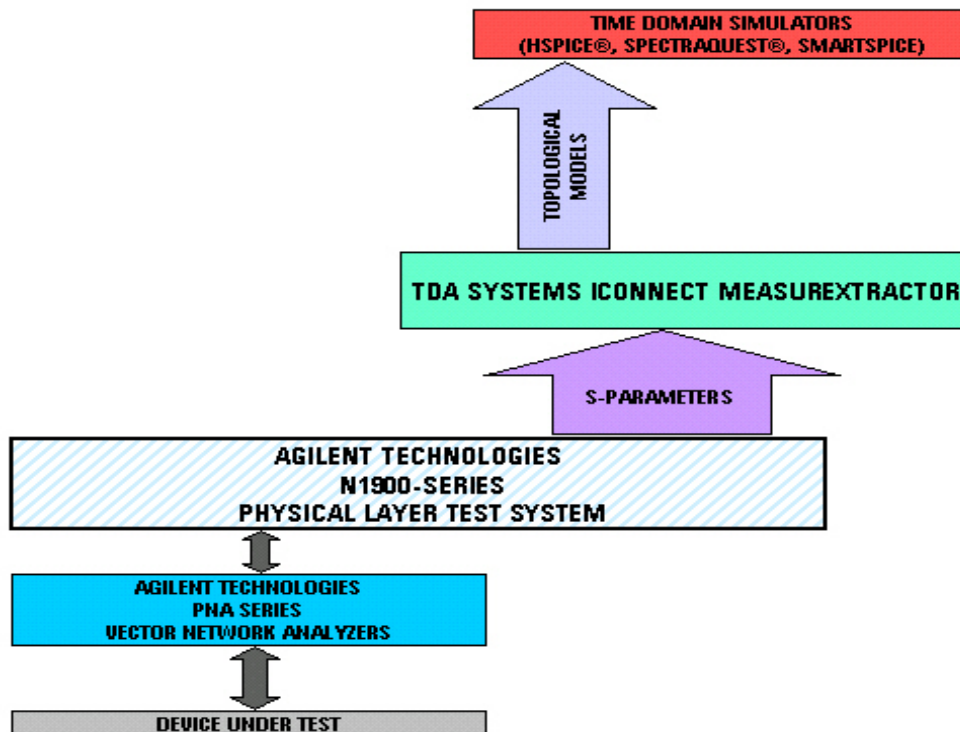


Figure 10. The first model extraction method used in this experiment used measurements from a VNA, then exported the 4-port S-parameters from PLTS directly into MeasureXtractor. A topological model was then exported from MeasureXtractor into Hspice

Partitioning the Impedance Profile

Optimized Hspice Models must be created by compiling measurement based model schematics in the model extraction tool to make Hspice TDR/T simulations and iterations to refine the match of the measurements as extracted from the S4P files. Both single-ended, differential, even and odd mode simulations can be conducted at the discretion of the engineer. Most importantly, the engineer must check the integrity of all DUT components before diving into model extraction and optimization. For this case, two separate coaxial cables were presumed to match physically and electrically. Both differential leg TDR voltage waveforms were checked for faults before being superimposed as differential or odd/even impedance profiles.

Behavioral S-parameter measurements were exported into the model extraction tool to construct Hspice topological models. Effectively, S-parameters are “time gated” and “re-time gated” in IConnect until Hspice topological simulations match the measurements. Fortunately this iterative optimization sequence requires only PC work and is easily automated. Both impedance and lossy models were constructed using this methodology. Hspice fitted simulations to the TDR, TDT and S-parameter data enabling the authors to divide and conquer complex modeling applications.

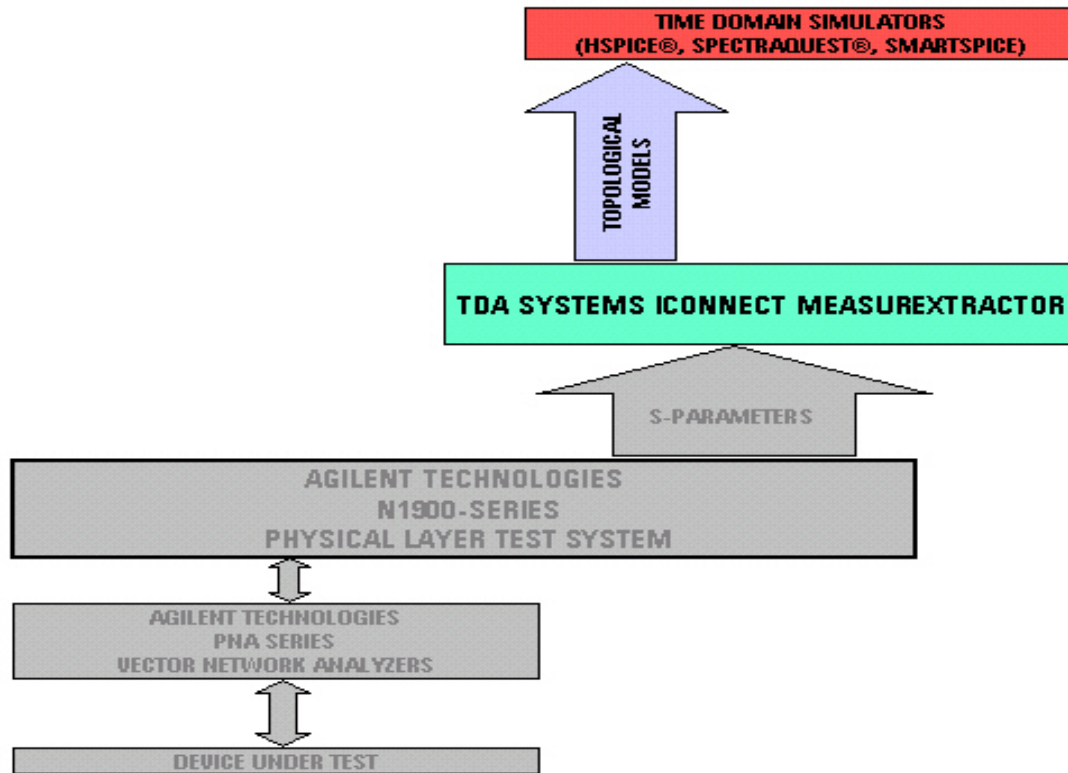


Figure 11. Behavioral S-parameter measurements were exported into the model extraction tool to construct Hspice topological models.

Correlating Measurements and Models

As seen on the upper left hand side of Figure 12, the VNA measurement of Input Differential Insertion Loss (SDD21) correlates well with the upper right hand side modeled Input Differential Insertion Loss (SDD21) of the model extraction tool that imported the 4-port S-parameter file from PLTS. Furthermore, the lower left hand side eye diagram simulation using the virtual pattern generator of PLTS and the lower right hand side of the MeasureXtractor eye diagram simulation matches quite well with each other. In both eye diagram simulations, a similar algorithm was used in each case. The 4-port S-parameter data was used to create an impulse response of the ChannelPlane device. The impulse response was then convolved with an arbitrary binary sequence to achieve a simulated eye diagram. The resultant eye diagram shows the extremely high performance of the ChannelPlane exceeding 40Gb/s. Future experiments will attempt correlation to eye diagrams measured from a Digital Communications Analyzer and 40Gb/s PRBS pattern generator.

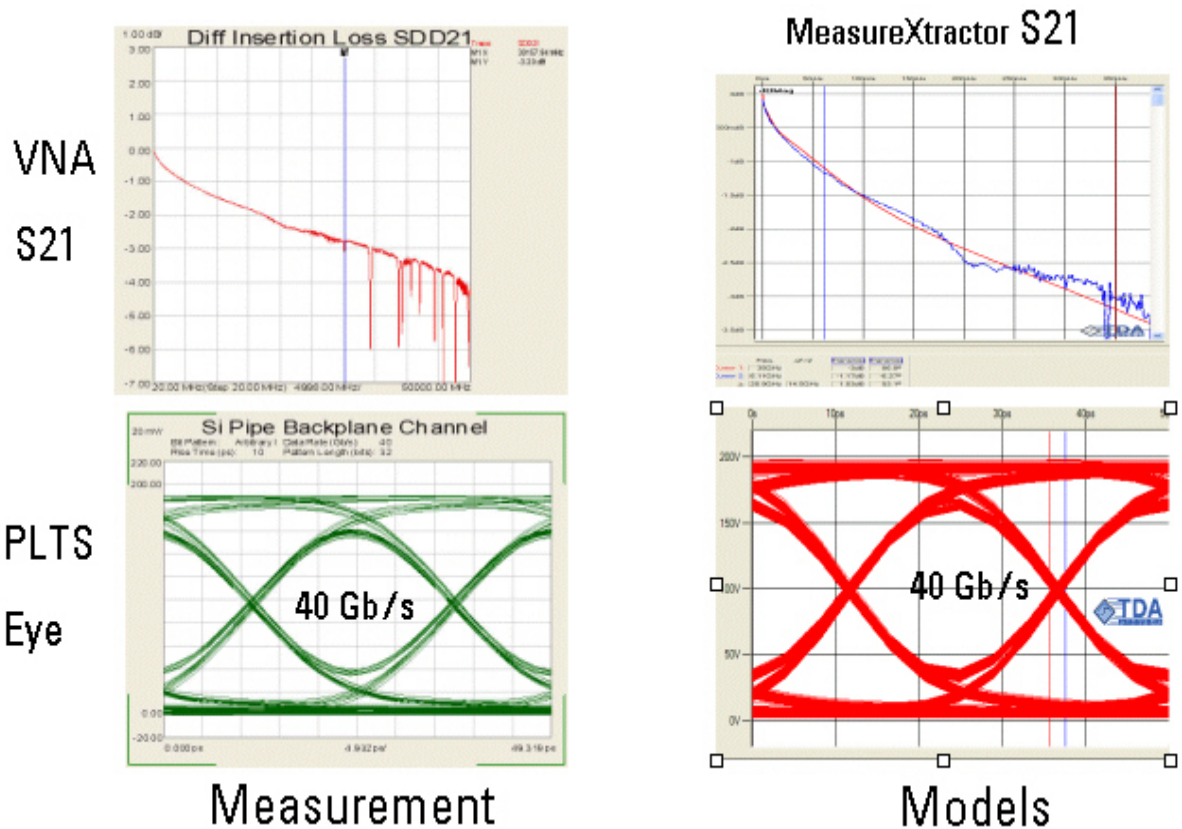


Figure 12. Correlation of Input Differential Insertion Loss (SDD21) and 40Gb/s eye diagram was very good between measurement and simulation.

Hspice Subcircuit Model for Backplane Only

An Hspice W model was extracted from one leg of a backplane differential cable, which had absolutely no physical or electrical defects out to 40 GHz. The Hspice W model is shown in Figure 13 in RLGC format. It includes skin effect resistance ($R_{ac}=133 \mu\text{-ohms}$)

per root Hertz) and dielectric loss ($G_{ac}=213$ f-Siemens per Hertz.) with good agreement between measured and modeled S parameters; predicting a valid 40 Gb/s eye pattern well correlated to VNA/PLTS test data as shown in Figure 12. However the 2nd leg of this backplane pair had internal break; exhibiting a 2 ohm impedance dip as shown in Figure 14. The W model for this broken leg was the same as the good leg except for a slight increase in dielectric loss (Gd). It can be concluded that losses associated with the break are shunt losses; linearly dependant with frequency like dielectric loss.

- `.subckt Lossy_Line_34_wire_30in port1 port2 gnd_`
- `W1 N=1 port1 gnd_ port2 gnd_`
`RLGCMODEL=Lossy_Line_34_wire_30in_Model L=1.0`
- `* RLGC values for W element`
- `.MODEL Lossy_Line_34_wire_30in_Model W MODELTYPE=RLGC N=1`
- `+ Lo=1.66268e-007`
- `+ Co=6.86542e-011`
- `+ Ro=0.102`
- `+ Go=1.14e-006`
- `+ Rs=0.000133`
- `+ Gd=2.13333e-013`
- `.ends`

Figure 13. Hspice subcircuit model of backplane cable without flush mount connector

When Flush Mount Connectors were sliced into the backplane cable and re-tested on the VNA, no change in skin effect resistance was detected in either leg of the differential backplane cable. Only an increase in dielectric loss (Gd) was detected. The flush mount connector appears to behave like a cable break as shown in Figure 15.

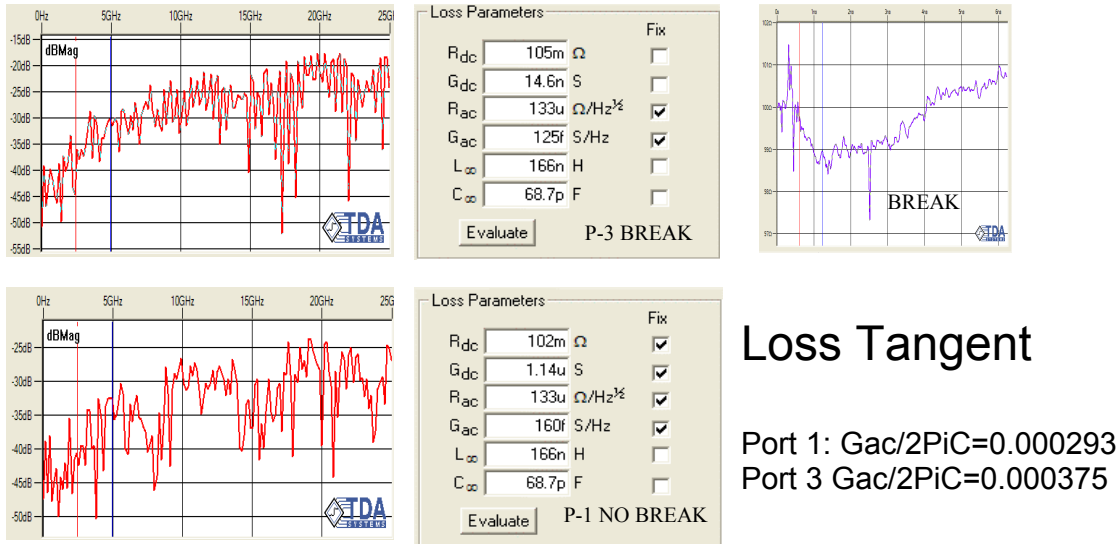


Figure 14. Backplane cable assembly lossy models shows loss tangent with impedance discontinuity due to cable break on one side of differential pair.

Discontinuities: Flush Connector versus Cable Break

The impedance profile of a cable break shown in Figure 14 is very similar to the impedance profile of a flush mount connector shown in Figure 15. Both are modeled as ~2 ohm capacitive discontinuity at a distance from the end of the cable SMA termination. The objective of the flush mount connection is to maintain a constant impedance through the connection. The observed capacitance discontinuity for both is in the order of 1/2 pf. The only obvious difference is that there are two flush mount connectors or twice the insertion loss and an elevated return loss due to two breaks rather than a single break.

The Impedance profile accuracy of this capacitance discontinuity could be an issue because the connector slice could be only 5 mils wide. The VNA test step risetime was 10ps with a propagation velocity in the cable being 120 ps/in. The model extraction tool resolves an impedance profile to ~1/10 of the risetime or ~1 ps. That translates to 1/120 of an inch of maximum resolution or >10 mils. That means cursor placements used to measure capacitance on the capacitance impedance profile could have resolution issues in the 1-5 mil range. So its presumed that 400 ff was a maximum and it could be as low as 100 ff. Hspice iterated the capacitance until a return loss simulation matched the measurement.

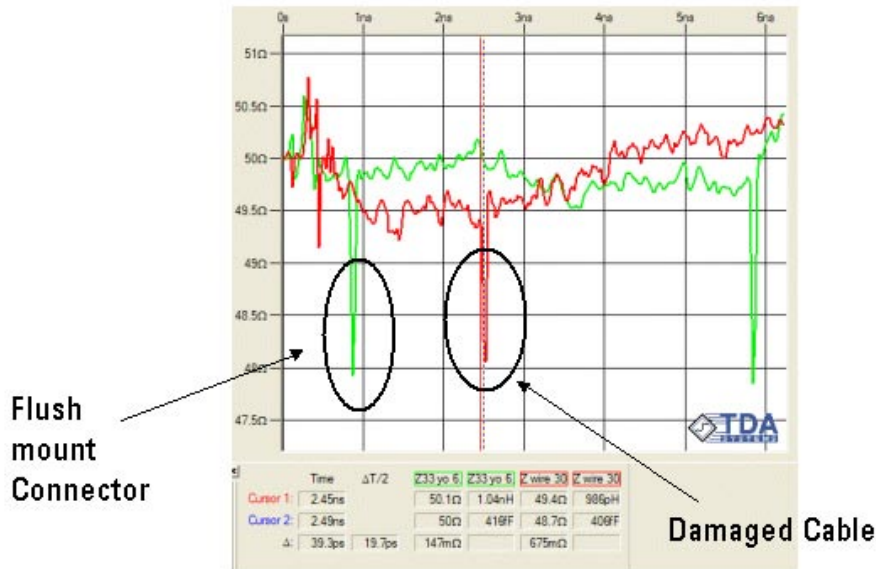


Figure 15. Impedance discontinuities from two different physical structures can look very similar. However, the intuitive nature of TDR's helps discriminate between and break in the cable and the flush mount connector.

HSpice Subcircuit Model for Backplane Flush Connector

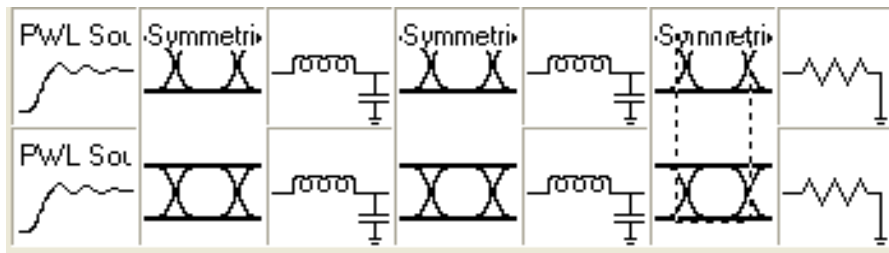
Connectorized cable modeling yielded a similar Hspice model with the same skin effect resistance R_s of 111u ohms per root Hertz. This was extracted on the 2nd VNA 30 GHz test with connector sliced into the previously test cables. However, G_d increased significantly due to the flush mount connectors. Again, the model extraction tool S-parameters agreed with VNA measurements. But the eye pattern was degraded over the previous measurements on the cable only. Was the degradation solely related to the flush mount connectors? Since both the eye height and jitter changed less than 20%, it was presumed to be the connectors until proven otherwise. The increase in G_d can be observed with and without connectors by comparing G_d differences in the models shown in Figure 13 and Figure 16.

- .subckt Lossy_Line_butt_30in port1 port2 gnd_
- W1 N=1 port1 gnd_ port2 gnd
RLGCMODEL=Lossy_Line_butt_30in_Model L=1.0
- * RLGCMODEL values for W element
- .MODEL Lossy_Line_butt_30in_Model W MODELTYPE=RLGC N=1
- + Lo=1.62028e-007
- + Co=6.66083e-011
- + Ro=0.106434
- + Go=0
- + Rs=0.000111
- + Gd=2.86667e-013
- .ends

Figure 16. Hspice subcircuit model of backplane cable with flush mount connectors.

Model Optimization Schematic: Cable and Connector

The second VNA test simulation schematic is shown in figure 17 including both backplane cable and flush mount connectors. The simulation objective was to build both transmittance and reflectance (TDR/T) waveforms, convert them to S parameters and compare the simulations to the VNA measurements. For insertion loss, Hspice was used to overcome the test bandwidth difference between measurements with and without connectors. To do this, simulations 1st replicated return loss measurements by adjusting the connector capacitance until a match occurred. It was proven that the return loss was well below -10 dB. Therefore, the simulated TDT waveforms predict valid 40 Gb/s eye integrity using flush mount connectors. Hspice model simulations were fitted out to the 30 GHz including connector models with elevated return loss and easily extrapolated to Over 40 GHz. A valid 40 Gb/s eye was then generated with flush mount connectors



- Launch cable 3" cable flush X 24" cable flush X 3"
- 25ps Lossy 112ff Lossy 112ff

Figure 17. Differential Hspice schematic shows piecewise linear source, lossy transmission lines segments, lumped LC flush connector and termination.

Analyzing Connector Shunt Loss

Scaled W-models were interpolated by length from the VNA measurements and used to model a three inch launch and termination cables, as well as the 24 inch backplane cable. The partitioned schematic in figure 18 shows a TDR source, a 3in cable launch, a flush connector, a 2 foot backplane cable, another flush mount connector, and a 3 inch termination cable to 50 ohms. Several Hspice runs simulated the TDR voltage waveform with the objective to match a cable insertion and return losses with flush connectors. Only the dielectric loss had to be increased as shown in the model in Figure 16 as compared to the Model in Figure 13 without flush connectors

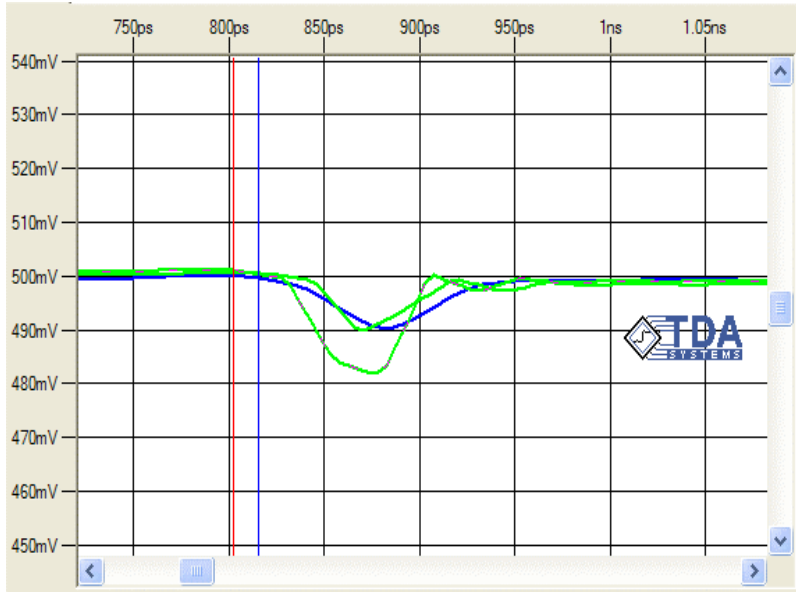


Figure 18. Simulated cable differential schematic for TDR leg waveforms showing connector capacitance discontinuity. Green simulation failed at 400 ff but passed at 112ff.

Analyzing Fringe Capacitance

Once shunt losses were accurately modeled, the connector impedance profile model was optimized by simulating a TDR waveform and adjusting the connector capacitance to best fit a 10mv TDR discontinuity as shown in Figure 18. Once fitted, the modeled TDR waveform was converted back to S-parameters and checked against the measured VNA S-parameters. Different connector capacitance values had to be iterated from a maximum of 400fF to refine the measurement accuracy. Even if the VNA measurement bandwidth was increased to 100 GHz, Hspice must still be used to overcome errors because the 3D fringe capacitance is physically very small. A -15 dB measured return loss was matched using a 112 fF connector capacitance; which then reached a maximum return loss of -12 dB at 36 GHz as shown in Figure 19.

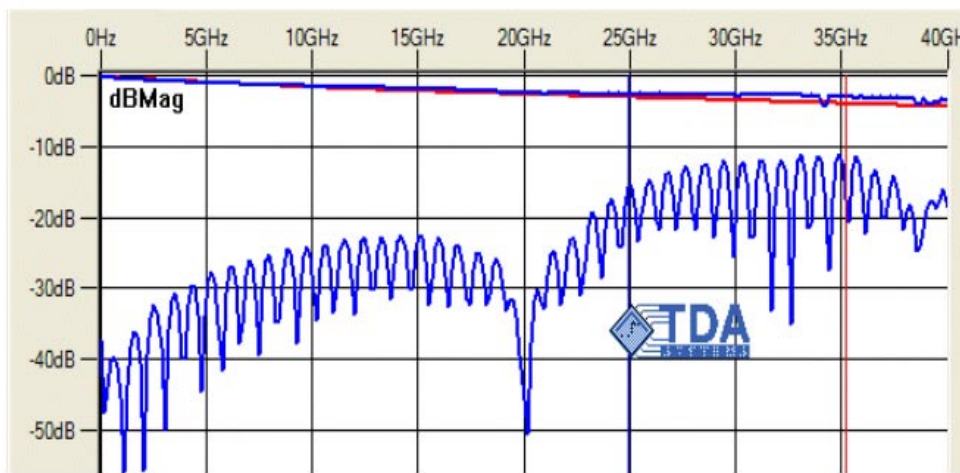


Figure 19. Simulated insertion loss (top) and return loss (bottom) for 30'' backplane cable assembly with 112femtoFarad connector.

Modeled S Parameters From Simulated TDR Waveforms

Simulated TDR waveforms were converted to S parameters and compared to VNA measurements. The modeled backplane/connector insertion loss (S21) shown in Red on figure 19 fits the attenuation measurements at a 25 GHz taken by the VNA with flush mount connectors on the 2nd test. The modeled backplane cable ONLY insertion loss in Blue fits the -3 dB at 35 GHz measurement taken by the VNA on the 1st test. With only a small return loss of -12 dB, the extrapolated insertion loss S-parameters appear valid out to 40 GHz. Given the small (5 ps) risetime degradation caused by the connectors, this model accurately “predicts” 40 Gb/s eye patterns as shown in Figure 20. If the backplane flush mount connector faces were polished to best match impedance, then return losses could reach -20 dB. Flush Mount connector technology therefore enhances copper interconnect performance out to 40 Gb/s; which is a most cost effective transition point to fiber optic hardware.

- Top shows eye without Connectors
 - Jitter PP: 2 ps
 - Eye height: 130mv
- Bottom shows eye with Connectors
 - Jitter PP: 2.4ps
 - Eye height: 90mv



Figure 20. Modeled eye diagrams with and without connectors.

Modeled Eye Diagram with and without connectors

The shunt losses in the connectors degraded the input risetime by only 5 ps and lowered the eye height by 10%. A 30 ps measured output risetime can be seen in the eye patterns starting at the left side (~10%) and reaching 30 ps at the center top (~90%). Still a 20 ps by 75 mv valid eye mask can be constructed inside this eye pattern. A key point is that the connector TDR discontinuity is short enough to minimize reflections sufficiently to not deteriorate eye opening. For this to occur, the return loss needs to be less than -10 dB. In conclusion, both a lossy and a capacitance models components are required to accurately simulate backplanes with flush mount connectors for both Insertion and return loss.

Conclusions

The “Polished” Cable Interface should be considered to minimize return loss in these experimental flush mount connectors. They were introduced on ends by precision slicing the cable as if it were a fiber optic connection with a goal to minimize discontinuity across the connection. If a copper interface were “polished” like fiber optic interface, then it might achieve a return loss as low as -20 dB.

The model to measurement correlation was excellent for risetime, eye patterns and S parameters with no issues identified. An S4P file extracted 40 GHz VNA backplane data set was used to model flush copper cable connectors; comparing S parameters with and without connectors by slicing them into a test cable. Hspice W model simulations fit VNA S parameters and TDR/T waveforms well for the backplane cable only. Yielding a 150mv eye height at 40 Gb/s with a 200 mv input and 2ps jitter.

Valid 40 Gb/s eye opening was achieved in backplane cables with connectors as modeled in Hspice.2nd VNA test evaluated the cable with connectors; transforming 30 GHz S parameters to TDR/T waveforms via 2nd S4P file. Results show a 5 ps connector I/O risetime degradation with return loss below -10dB; having no effect on the eye opening. But connector insertion loss did diminish eye height by ~10% due to shunt loss; which is linearly dependant on frequency like dielectric loss. A 10mv capacitance discontinuity was modeled by a 112ff capacitor placed 3 inches from the ends of the cable optimized by Hspice simulations. Further study of 3D fringe capacitance should be studied using 3D, time domain field solver to verify dimensions and refine model accuracy.

The advent of high-speed serial channels has driven the circuit topology to differential signaling. While this enables the inherent benefits of coupled pair of transmission lines, this adds new challenges for the signal integrity engineer. Measurement, model extraction and simulation are critical to an efficient design cycle and meeting time-to-market demands. It sometimes seems as if there are as many design tools as there design engineers, but the message is clear. New techniques that utilize measurement-based modeling are necessary for fully characterizing differential interconnects. It is now possible to use one measurement system for both time and frequency domain information that will quickly identify design flaws that ultimately degrade performance.